

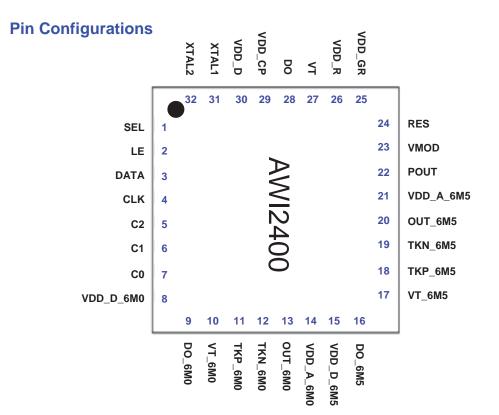
2.4GHz Wireless Transmitter

Product Description

The AWI2400 is a single chip and low power consumption transmitter designed for analog A/V sender and wideband digital FSK transmitter operating in the 2.4GHz ISM band. The transmitter IC consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a stereo audio modulator. The IC is provided in 32-lead QFN5X5 package and is designed to provide a fully functional FM/FSK transmitter.

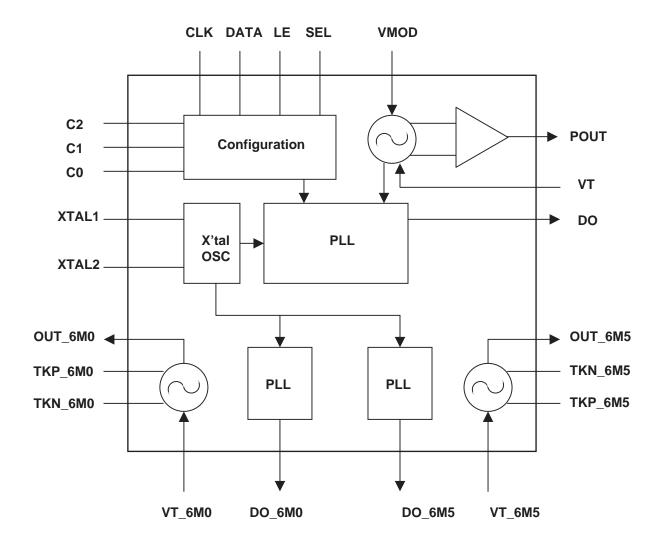
Main Features

- 3V power Supply
- 4 channel operation for analog A/V sender and digital FSK transmission applications
- Channel select by use of c0,c1 and c2 pins for a set of pre-defined frequencies
- Programmable user-defined channel frequencies by use of the 3-wire serial interface
- Two audio sub-carriers generated with PLL for high frequency accuracy and stability





Transmitter Block Diagram





Pin Descri tions

Pin No.	Name	Description	Equivalent Schematic
1	SEL	If PIN1 is unconnected (Internal pull high), the channel can be selected from a set of pre-defined channel frequencies by the settings of C0,C1,C2. If PIN1 is connected to GND, the channel frequencies can be programmed by an external MCU via the 3-wire serial interface, LE, DATA and CLK. See Note1	VDD
2	LE	Load Enable Input of 3-wire Series Interface PIN2 is enabled when SEL (PIN1) is connected to ground	2

Pin No.	Name	Description	Equivalent Schematic
3	DATA	DATA Input of 3-wire Series Interface PIN3 is enabled when SEL (PIN1) is connected to ground	3 — VDD — VD
4	CLK	CL CK Input of 3-wire Series Interface PIN is active when SEL (PIN1) is connected to ground	4

Pin No.	Name	Description	Equivalent Schematic
	C	Internal pull high, set PIN Low to select C 3 (2 0M) PIN is enabled when SEL (PIN1) is open	5
	C	Internal pull high, set PIN Low to select C 2 (2 32M) PIN is enabled when SEL (PIN1) is open See Note1	6 - VDD

Pin No.	Name	Description	Equivalent Schematic
	C	Internal pull high, set PIN Low to select C 1 (2 1 M) PIN is enabled when SEL (PIN1) is open See Note1	,
	DD D	Power supply for digital portion of .0M Audio Modulator Suggestion value of bypass capacitor C21 is 0.1u .	
	D	Charge Pump utput of .0M PLL	

Pin No.	Name	Description	Equivalent Schematic
	Т	.0M C Tuning oltage Control Input Typical range of t is 1.0 1	10
	ТКР	ne of the two connection pins for external Tan components of .0M C . Shorter traces for the interconnection of L and C are recommended. Suggestion values of L and C2 are 33u and 10p .	3mA • • • • • • • • • • • • • • • • • • •
	TKN	ne of the two connection pins for external Tan components of .0M C . Shorter traces for the interconnection of L and C are recommended. Suggestion values of L and C2 are 33u and 10p .	3mA 12



Pin No.	Name	Description	Equivalent Schematic
3	T	.0M Audio Modulator utput	To Do
4	DD A	Power supply for analog portion of .0M Audio Modulator. Suggestion values of bypass capacitor C2 is 0.1u .	
	DD D	Power supply for digital portion of . M Audio Modulator. Connect to DD A M0 (PIN1).	
	D	. M PLL Charge Pump utput	



Pin No.	Name	Description	Equivalent Schematic
	Т	. M C Tuning oltage Control Input Typical range of t is 1.0 1.	—— 17
	TKP	ne of the two connection pins for external Tan components of . M C . Shorter traces for the interconnection of L and C are recommended. Suggestion values of L and C2 are 33u and . p .	3mA 18
	TKN	ne of the two connection pins for external Tan components of . M C . Shorter traces for the interconnection of L and C are recommended. Suggestion values of L and C2 are 33u and . p .	3mA 19

Pin No.	Name	Description	Equivalent Schematic
	T	. M Audio Modulator utput	VDD 20
	DD A	Power supply for analog portion of . M Audio Modulator. Suggestion value of bypass capacitor C1 is 0.1u .	
	Р Т	G. Amplifier utput. Typical output power range is 2d m 1d m.	

Pin No.	Name	Description	Equivalent Schematic
3	D	M SK modulation signal input of 2. G C	
4	ES	External ias esistor for setting 2. G C bias current or optimal phase noise performance, a suggestion value of 1 is 12K	VDD T
	DD	Power supply for Guard ing. Suggestion values of bypass capacitors C and C are 0.1u and 100p.	
	DD	Power Supply for 2. G C . Connect to DD G (PIN2).	
	Т	C Tuning oltage Control Input, Connect to LP output	——— 27





Pin No.	Name	Description	Equivalent Schematic
	D	2. G PLL Charge Pump utput	28
	DD CP	Power supply for Charge Pump. Suggestion value of bypass capacitor C is 0.1u .	
3	DD P	Prescaler Power Supply Connect to DD CP (PIN2)	
3	TAL	ne of the two connection pins of external crystal	VDD 31
		See Note2	÷



Pin No.	Name	Description	Equivalent Schematic
3	TAL	ne of the two connection pins of external crystal See Note2	VDD 32



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Ma imum Rating

Parameter	Ma imum Rating	Units
Supply oltage (DD)		
Storage Temperature	-20 0	$^{\circ}\mathbb{C}$

Note This device is ESD sensitive. andling and assembly of this device should only be done at proper ESD protection environment.

Electrical C aracteristics

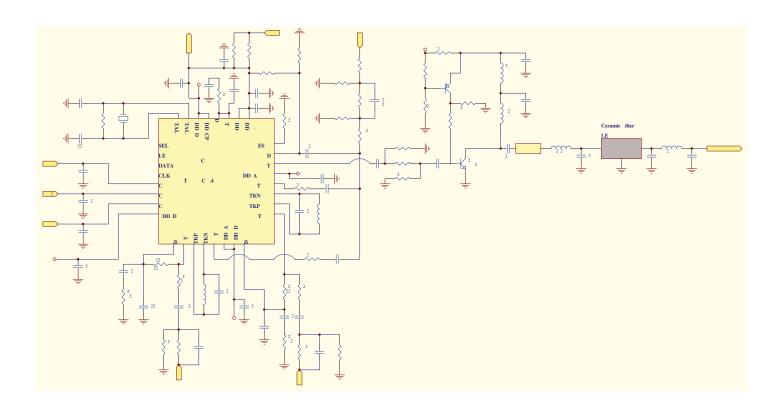
Parameter	Descri tion	Min.	Τ.	Ma .	Unit
peration Temperature		-10		0	°C
Supply oltage		3.0		3.	
Current Consumption			32		mA
utput Power		-2	1	2	d m
eference requency					М
Crystal Accruacy			30		ppm
peration requency (SEL igh)		2 1 , 2 32, 2 0, 2		М	
.0M Audio Modulator utput Level		2.		3	pp
. M Audio Modulator utput Level		2.		3	рр





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A lication Circuit 6 0TX Block Diagram



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Note

1. C annel Selection SEL C2 C1 C0 PIN1 PIN5 PIN6 PIN

If SEL(PIN1) is unconnected (internal pull high) then connect **C2**, **C1**, **C0** to a 3 pins DIP switch to select the channel according to Table1.

Note **C2**, **C1**, **C0** are internal pull high and are enabled when connected to ground. hen more than one pins are low, the lowest channel is the selected one (e.g. C 1 is selected when both C0 and C1 are low). If no pins are connected to ground, C is the default channel.

С	requenc	C	С	C
	4 4			
	43			
3	4			
4	4			

Table1

. TAL PN3 an TAL PN3

igure.1 shows the recommended crystal oscillator circuit diagram.The resistor $\,$ f is connected in parallel with the crystal and between the input and output of the inverter to provide a negative DC feedbac . Usually, the range of its resistance value is $\,$ 00K Ω $\,$ 2 $\,$ Ω

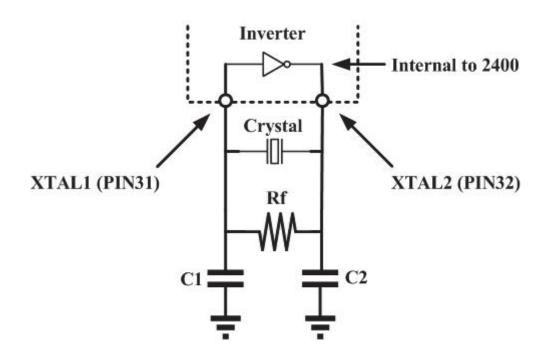
The capacitors C₁ and C₂ provide the necessary load capacitance for resonating the crystal. Their values can be determined by the following equation

$$C_L = \frac{C_1 + C_2}{C_1 + C_2} + C_S$$

where CL is the load capacitance of the crystal whose value can be obtained from the data sheet provided by the crystal manufacturer and Cs is the stray capacitance on the printed circuit board. A typically value of Cs is 0.3 0. p . Larger values of C1and C2 increases frequency stability but decreases loop gain. Suggestion values of C1, C2 and $\,$ f are 22p $\,$, 30p $\,$ and 1M Ω $\,$ respectively



Note

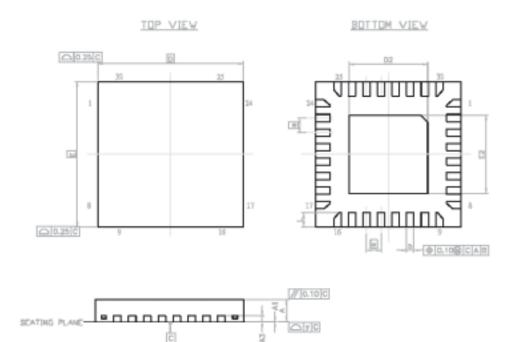


igure1



Package Information

N 2 Outline Dimensions



SYMBOL	NDI ZN AMIO			DIMENSION (MIL)			
	MIN.	NOM.	MAX.	MIN.	NDH.	MAX.	
A	0.70	0.75	0.80	27.6	29.5	31.5	
A1	0	0.02	0.05	0	0.8	2.0	
A3	0.20 REF			9.8 REF			
h	0.18	0.25	0.30	7.1	9.8	11.8	
D	5.00 BSC			196.9 BSC			
D5	2.60	2.70	2.80	102.4	106.3	110.2	
Ε	5.00 BSC			196.9 BSC			
E2	2.60	2.70	2.80	102.4	106.3	110.2	
8	0.50 BSC			19.7 BSC			
L	0.30	0.40	0.50	11.8	15.7	19.7	
У	0.10			3.9			